IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Original) A method of analyzing circuits, said method comprising:

creating a set of interpolated models for transistors;

creating a set of characterized models for said transistors;

analyzing said transistors within a netlist for matches in said set of characterized models; and

providing a choice of using the matched characterized models or one of said interpolated models in designing said circuits.

2. (Original) The method of claim 1, further comprising:

schematically simulating a custom circuit;

back annotating to a schematic circuit which of said transistors use direct-fit models and which of said transistors are interpolated;

determining whether said transistors are in any of cutoff, saturation, static linear, and dynamic linear mode during simulation of said custom circuit;

extracting said saturation and dynamic linear mode transistors;

back annotating said netlist to a schematic with a predetermined device state; and

performing sensitivity analysis on saturation and dynamic linear mode transistors.

3. (Original) The method of claim 2, wherein said sensitivity analysis determines which transistors most affect design criteria.

4. (Original) The method of claim 3, wherein once said transistors most affecting design criteria are identified, said transistors are specified with a closest characterized model in a most to least critical order to fit most of said design criteria into a direct fit simulation.

5. (Original) The method of claim 1, wherein said interpolated models and said characterized models comprise parallel sets of models to characterize transistor sizes and parameters including electrical and environmental conditions.

6. (Currently Amended) The method of claim 1, further comprising:

recognizing transistors in said netlist which may be simulated with said characterized models;

providing feedback information relating to which transistors use said characterized models;

analyzing said netlist to determine which transistors using said interpolated models would benefit from using said characterized models;

simulating changes to said netlist to facilitate switching to said characterized models; and

back annotating a series of scenarios to a circuit design layout framework for designer selection.

7. (Currently Amended) The method of claim 6, further comprising:

using information tags for propagation to said circuit design layout framework for each transistor;

selecting the propagated information tags in netlist parasitic extraction; and

simulating the ~~parasitic netlist~~ netlist parasitic extraction to ensure post-layout integrity.

8. (Original) A method of designing electrical circuits, said method comprising:

creating a set of interpolated models for devices;

creating a set of direct fit models for said devices;

analyzing said devices within a netlist for matches in said set of direct fit models; and

providing a choice of using the matched direct fit models or one of said interpolated models in designing said circuits.

9. (Original) The method of claim 8, further comprising:

schematically simulating a custom circuit;

back annotating to a schematic circuit which of said devices use direct-fit models and which of said devices are interpolated;

determining whether said devices are in any of cutoff, saturation, static linear, and dynamic linear mode during simulation of said custom circuit;

extracting said saturation and dynamic linear mode devices;

back annotating said netlist to a schematic with a predetermined device state; and

performing sensitivity analysis on saturation and dynamic linear mode devices.

10. (Original) The method of claim 9, wherein said sensitivity analysis determines which devices most affect design criteria.

11. (Original) The method of claim 10, wherein once said devices most affecting design criteria are identified, said devices are specified with a closest direct fit model in a most to least critical order to fit most of said design criteria into a direct fit simulation.

12. (Original) The method of claim 8, wherein said interpolated models and said direct fit models comprise parallel sets of models to characterize transistor sizes and parameters including electrical and environmental conditions.

13. (Currently Amended) The method of claim 8, further comprising:

recognizing devices in said netlist which may be simulated with said direct fit models;

providing feedback information relating to which devices use said direct fit models;

analyzing said netlist to determine which devices using said interpolated models would benefit from using said direct fit models;

simulating changes to said netlist to facilitate switching to direct fit models; and

back annotating a series of scenarios to a circuit design layout framework for designer selection.

14. (Currently Amended) The method of claim 13, further comprising:

using information tags for propagation to said circuit design layout framework for each transistor;

selecting the propagated information tags in netlist parasitic extraction; and

simulating the ~~parasitic netlist~~ netlist parasitic extraction to ensure post-layout integrity.

15. (Original) A program storage device readable by computer, tangibly embodying a program of instructions executable by said computer to perform a method of analyzing and designing circuits, said method comprising:

creating a set of interpolated models for transistor devices;

creating a set of characterized models for said transistor devices;

analyzing said transistor devices within a netlist for matches in said set of characterized models; and

providing a choice of using the matched characterized models or one of said interpolated models in designing said circuits.

16. (Original) The program storage device of claim 15, wherein said method further comprises:

schematically simulating a custom circuit;

back annotating to a schematic circuit which of said transistors use direct-fit models and which of said transistor devices are interpolated;

determining whether said transistor devices are in any of cutoff, saturation, static linear, and dynamic linear mode during simulation of said custom circuit;

extracting said saturation and dynamic linear mode transistor devices;

back annotating said netlist to a schematic with a predetermined device state; and

performing sensitivity analysis on saturation and dynamic linear mode transistor devices.

17. (Original) The program storage device of claim 16, wherein said sensitivity analysis determines which transistor devices most affect design criteria.

18. (Original) The program storage device of claim 17, wherein once said transistor devices most affecting design criteria are identified, said transistor devices are specified with a closest characterized model in a most to least critical order to fit most of said design criteria into a direct fit simulation.

19. (Original) The program storage device of claim 15, wherein said interpolated models and said characterized models comprise parallel sets of models to characterize transistor device sizes and parameters including electrical and environmental conditions.

20. (Currently Amended) The program storage device of claim 15, wherein said method further comprises:

recognizing transistor devices in said netlist which may be simulated with said characterized models;

providing feedback information relating to which transistor devices use said characterized models;

analyzing said netlist to determine which transistor devices using said interpolated models would benefit from using said characterized models;

simulating changes to said netlist to facilitate switching to said characterized models; and

back annotating a series of scenarios to a circuit design layout framework for designer selection.

21. (Currently Amended) The program storage device of claim 20, wherein said method further comprises:

using information tags for propagation to said circuit design layout framework for each transistor device;

selecting the propagated information tags in netlist parasitic extraction; and

simulating the ~~parasitic netlist~~ netlist parasitic extraction to ensure post-layout integrity.

22. (New) A method of analyzing circuits, said method comprising:

creating a set of interpolated models for transistors;

creating a set of characterized models for said transistors;

analyzing said transistors within a netlist for matches in said set of characterized models;

providing a choice of using the matched characterized models or one of said interpolated models in designing said circuits; and

performing sensitivity analysis on said transistors.